BY29GM2G

2G BIT Parallel NOR FLASH

Distinctive Characteristics

- BY29GM2GFS is a dual die stack of two BY29G1GFS die
- Single 3V read/program/erase (2.7-3.6 V)
- Enhanced VersatileI/O™ control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 to V_{CC}
- 8-word/16-byte page read buffer
- 32-word/64-byte write buffer reduces overall programming time for multiple-word updates
- Secured Silicon Sector region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number
  - Can be programmed and locked at the factory or by the customer
- Uniform 64 Kword/128 Kbyte Sector Architecture
  - BY29GM2GFS: two thousand forty-eight sectors
- 100,000 erase cycles per sector typical
- 20-year data retention typical
- Offered Packages
  - 56-pin TSOP
  - 64-ball Fortified BGA
- Write operation status bits indicate program and erase operation completion
- Unlock Bypass Program instruction to reduce programming time
- Support for CFI (Common Flash Interface)
- Persistent and Password methods of Advanced Sector Protection
- WP#/ACC input
- Hardware reset input (RESET#) resets device
- Ready/Busy# output (RY/BY#) detects program or erase cycle completion

Performance Characteristics

Maximum Read Access Times (ns)					
Density	**Voltage Range (1)**	**Random Access Time (t_{ACC})**	**Page Access Time (t_{PACC})**	**CE# Access Time (t_{CE})**	**OE# Access Time (t_{OE})**
2 Gb	Regulated V_{CC}	110	25	110	25
	Full V_{CC}	120		120	
	VersatileIO V_{IO}	130		130	

Note

1. *Access times are dependent on V_{CC} and V_{IO} operating ranges. See Order Information for further details.*
   Regulated V_{CC}: V_{CC} = 3.0–3.6 V.
   Full V_{CC}: V_{CC} = V_{IO} = 2.7–3.6 V.
   VersatileIO V_{IO}: V_{IO} = 1.65–V_{CC}, V_{CC} = 2.7–3.6 V.
2. *Contact a sales representative for availability*

Current Consumption (typical values)	
Random Access Read (*f* = 5 MHz)	30 mA
8-Word Page Read (*f* = 10 MHz)	1 mA
Program/Erase	50 mA
Standby	100 µA

Program & Erase Times (typical values)	
Single Word Programming	60 µs
Effective Write Buffer Programming (V_{CC}) Per Word	15 µs
Effective Write Buffer Programming (V_{HH}) Per Word	13.5 µs
Sector Erase Time (64 Kword Sector)	0.5 s

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1. Description

The **BY29GM2GFS** is flash product fabricated on ETOX 50 nm process technology. These devices offer a fast page access time of 25 ns with a corresponding random access time as fast as 110 ns. They feature a Write Buffer that allows a maximum of 32 words/64 bytes to be programmed in one operation, resulting in faster effective programming time than standard programming algorithms. This makes these devices ideal for today's embedded applications that require higher density, better performance and lower power consumption.

The **BY29GM2GFS** is a dual die stack of two **BY29G1GFS** die. For detailed specifications, refer to the discrete die datasheet provided in **BY29G1GFS**.

Figure 1. Logic diagram

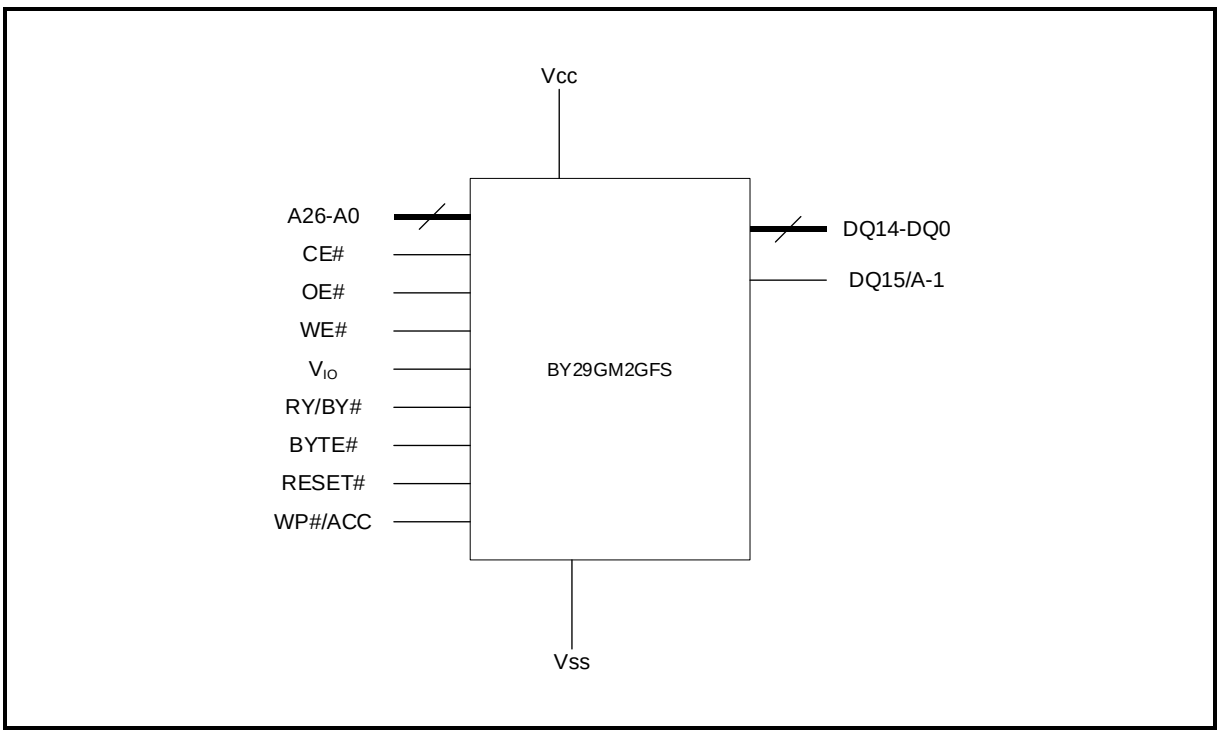
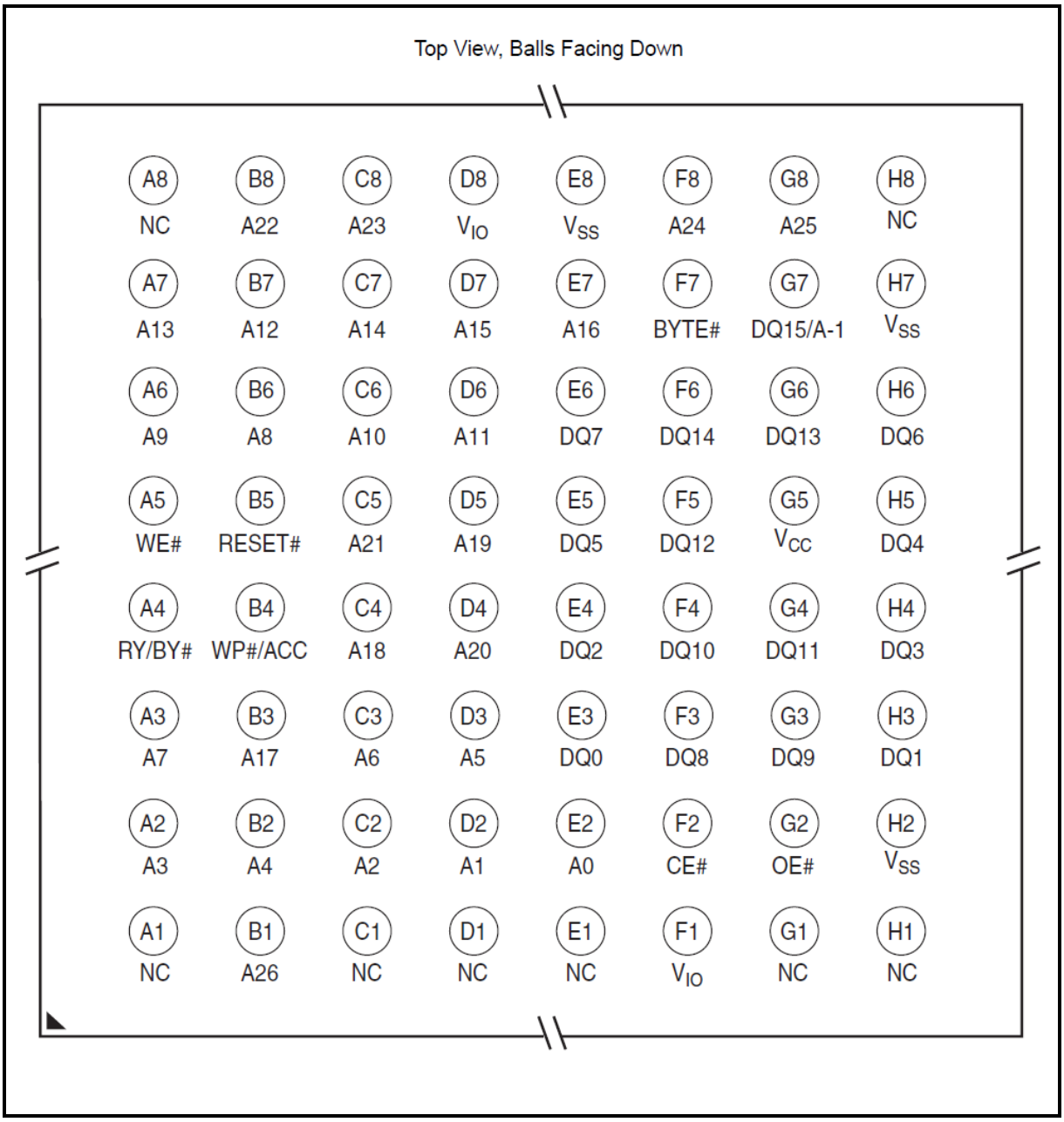


Figure 2. Pin Configuration



2. Signal Description

Table 1. Signal Names

Symbol	Type	Description
A26-A0 (Note 1)	Input	Address lines for BY29GM2GFS
DQ14–DQ0	I/O	Data input/output
DQ15/A-1	I/O	DQ15: Data input/output in word mode A-1: LSB address input in byte mode
CE#	Input	Chip Enable
OE#	Input	Output Enable
WE#	Input	Write Enable
V_{CC}	Supply	Device Power Supply
V_{IO}	Supply	Versatile IO Input
V_{SS}	Supply	Ground
NC	No Connect	Not connected internally
RY/BY#	Output	Ready/Busy. Indicates whether an Embedded Algorithm is in progress or complete. At V_{IL}, the device is actively erasing or programming. At High Z, the device is in ready
BYTE#	Input	Selects data bus width. At V_{IL}, the device is in byte configuration and data I/O pins DQ0-DQ7 are active and DQ15/A-1 becomes the LSB address input. At V_{IH}, the device is in word configuration and data I/O pins DQ0-DQ15 are active
RESET# (Note 2)	Input	Hardware Reset. Low = device resets and returns to reading array data
WP#/ACC	Input	Write Protect/Acceleration Input. At V_{IL}, disables program and erase functions in the outermost sectors. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. Should be at V_{IH} for all other conditions. WP# has an internal pull-up; when unconnected, WP# is at V_{IH}

Note:

1. *A26 can be used to select the die to be operated. For example, if A26 = 0, all operations are only valid for the 0th die (except for hardware reset, not related to A26), that is, if A26 = 0, can only read/program/erase /suspend/resume the array/Secured Silicon Sector/register/PPB/DYB/password, etc. of the 0th die. Chip erase is also only valid for 0th die. Can only read Write Operation Status of 0th die. And can only enter Autoselect, CFI mode of 0th die.*
   Therefore, in each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.
2. *RESET# is valid for the two die at the same time.*

3. Sector Addresses

Table 2. Sector Addresses of BY29GM2GFS

Memory Density	Big Block (256Kword/512Kbyte)	Sector (64Kword/128Kbyte)	Address Range
2Gbit	Big Block 0	Sector 0	0000000h-000FFFFh
		:	:
		Sector 3	0030000h-003FFFFh
	:	:	:
	Big Block 511	Sector 2044	7FC0000h-7FCFFFFh
		:	:
		Sector 2047	7FF0000h-7FFFFFFh

Note:

3. *Big Block = Uniform Big Block, and the size is 256 Kword/ 512Kbyte.*
4. *Sector = Uniform Sector, and the size is 64K word/128K byte.*

4. Instructions Description

4.1 Instruction Definitions

4.1.1 Memory Array Instruction Definitions, x16

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Single word program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (7)		6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
Program Buffer to Flash (Confirm)		1	SA	29										
Write-to-Buffer-Abort Reset		3	555	AA	2AA	55	555	F0						
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Erase Suspend/Program Suspend		1	XXX	B0										
Erase Resume/Program Resume		1	XXX	30										
Reset		1	XXX	F0										
Unlock Bypass	Enter	3	555	AA	2AA	55	555	20						
	Read (6)	1	RA	RD										
	Single word program	2	XXX	A0	PA	PD								
	Write to Buffer (7)	6	SA	25	SA	WC	WBL	PD						
	Program Buffer to Flash (Confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	555	AA	2AA	55	555	F0						
	Sector Erase	2	XXX	80	SA	30								
	Chip Erase	2	XXX	80	XXX	10								
	Reset	2	XXX	90	XXX	00								
Secured Silicon Sector	Secured Silicon Sector Entry	3	555	AA	2AA	55	555	88						
	Read (6)	1	RA	RD										
	Single word program	4	555	AA	2AA	55	555	A0	PA	PD				
	Write to Buffer (7)	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD
	Program Buffer to Flash (Confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	555	AA	2AA	55	555	F0						
	Secured Silicon Sector Exit	4	555	AA	2AA	55	555	90	XX	00				
Autoselect (8)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	01				
	Device ID	6	555	AA	2AA	55	555	90	X01	227E	X0E		X0F	
	Sector Protect Verify	4	555	AA	2AA	55	555	90	[SA]X02					

	Secure Device Verify	4	555	AA	2AA	55	555	90	X03					
	Reset	1	XXX	F0										
CFI	CFI Query (9)	1	55	98										
CFI	Read (6)	1	RA	RD										
CFI	Reset	1	XXX	F0										

Legend

X = Don't care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first. SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
WC = Word Count is the number of write buffer locations to load minus 1.

Note

1. All values are in hexadecimal.
2. All bus cycles are write cycles unless otherwise noted.
3. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
4. In each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.
5. Address bits A_{MAX}:A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
6. No unlock or instruction cycles required when reading array data.
7. Depending on the number of words written, the total number of cycles may be from 6 to 37.
8. The fourth, fifth, and sixth cycles of the autoselect instruction sequence are read cycles.
9. Instruction is valid when device is ready to read array data or when device is in autoselect mode.

4.1.2 Sector Protection Instruction Definitions, x16

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First/ Seventh		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Instruction Set Entry	3	555	AA	2AA	55	555	40						
	Program	2	XXX	A0	XXX	DATA								
	Read	1	00	RD										
	Instruction Set Exit	2	XXX	90	XXX	00								
Password Protection	Instruction Set Entry	3	555	AA	2AA	55	555	60						
	Password Program (6)	2	XXX	A0	PWAx	PWDx								
	Password Read (7)	4	00	PWD0	01	PWD 1	02	PWD 2	03	PWD 3				
	Password Unlock (7)	7	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			00	29										
	Instruction Set Exit	2	XXX	90	XXX	00								
Global Non-Volatile	PPB Instruction Set Entry	3	555	AA	2AA	55	555	C0						
	PPB Program	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read	1	SA	RD (0)										
	PPB Instruction Set Exit	2	XXX	90	XXX	00								
Global Volatile Freeze	PPB Lock Instruction Set Entry	3	555	AA	2AA	55	555	50						
	PPB Lock Set	2	XXX	A0	XXX	00								
	PPB Lock Status Read	1	XXX	RD (0)										
	PPB Lock Instruction Set Exit	2	XXX	90	XXX	00								
Volatile	DYB Instruction Set Entry	3	555	AA	2AA	55	555	E0						
	DYB Set	2	XXX	A0	SA	00								
	DYB Clear	2	XXX	A0	SA	01								
	DYB Status Read	1	SA	RD (0)										
	DYB Instruction Set Exit	2	XXX	90	XXX	00								

Legend

X = Don't care RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector. PWD = Password
PWDx = Password word0, word1, word2, and word3.
Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Note

1. All values are in hexadecimal.
2. All bus cycles are write cycles unless otherwise noted.
3. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
4. In each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.
5. Address bits A_{MAX}: A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.)
6. For PWDx, only one portion of the password can be programmed per each "A0" instruction.
7. Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.

4.1.3 Memory Array Instruction Definitions, x8

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (6)		1	RA	RD										
Single word program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer 7)		6	AAA	AA	555	55	SA	25	SA	WC	WBL	PD	WB L	PD
Program Buffer to Flash (confirm)		1	SA	29										
Write-to-Buffer-Abort Reset		3	AAA	AA	555	55	AAA	F0						
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AA A	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Erase Suspend/Program Suspend		1	XXX	B0										
Erase Resume/Program Resume		1	XXX	30										
Reset		1	XXX	F0										
Unlock Bypass	Enter	3	AAA	AA	555	55	AAA	20						
	Read (6)	1	RA	RD										
	Single word program	2	XXX	A0	PA	PD								
	Write to Buffer (7)	6	SA	25	SA	WC	WBL	PD						
	Program Buffer to Flash (confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	AAA	AA	555	55	AAA	F0						
	Sector Erase	2	XXX	80	SA	30								
	Chip Erase	2	XXX	80	XXX	10								
	Reset	2	XXX	90	XXX	00								
Secured Silicon Sector	Secured Silicon Sector Entry	3	AAA	AA	555	55	AAA	88						
	Read (6)	1	RA	RD										
	Single word program	4	AAA	AA	555	55	AAA	A0	PA	PD				
	Write to Buffer(7)	6	AAA	AA	555	55	SA	25	SA	WC	WBL	PD	WB L	PD
	Program Buffer to Flash (confirm)	1	SA	29										
	Write-to-Buffer-Abort Reset	3	AAA	AA	555	55	AAA	F0						
	Secured Silicon Sector Exit	4	AAA	AA	555	55	AAA	90	XX	00				
Autoselect (8)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID	6	AAA	AA	555	55	AAA	90	X02	XX7 E	X1C		X1E	(8)
	Sector Protect Verify	4	AAA	AA	555	55	AAA	90	[SA]X04					
	Secure Device Verify	4	AAA	AA	555	55	AAA	90	X06					
	Reset	1	XXX	F0										
CFI	CFI Query (9)	1	AA	98										
	Read (6)	1	RA	RD										
	Reset	1	XXX	F0										

Legend

X = Don’t care
RA = Address of the memory to be read.
RD = Data read from location RA during read operation.
PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.
PD = Data to be programmed at location PA. Data latches on the rising edge of the WE# or CE# pulse, whichever happens first. SA = Address of the sector to be verified (in autoselect mode) or erased. Address bits Amax–A16 uniquely select any sector.
WBL = Write Buffer Location. The address must be within the same write buffer page as PA.
WC = Word Count is the number of write buffer locations to load minus 1.

Note

1. All values are in hexadecimal.
2. All bus cycles are write cycles unless otherwise noted.
3. Data bits DQ15-DQ8 are don’t cares for unlock and instruction cycles.
4. In each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.
5. Address bits A_{MAX}:A12 are don’t cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.).
6. No unlock or instruction cycles required when reading array data.
7. Depending on the number of words written, the total number of cycles may be from 6 to 69
8. The fourth, fifth, and sixth cycles of the autoselect instruction sequence are read cycles.
9. Instruction is valid when device is ready to read array data or when device is in autoselect mode.

4.1.4 Sector Protection Instruction Definitions, x8

Instruction (Notes)		Cycles	Bus Cycles (Notes 1–5)											
			First/ Seventh		Second/ Eighth		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register	Instruction Set Entry	3	AAA	AA	555	55	AAA	40						
	Bits Program	2	XXX	A0	XXX	DATA								
	Read	1	00	RD										
	Instruction Set Exit	2	XXX	90	XXX	00								
Password Protection	Instruction Set Entry	3	AAA	AA	555	55	AAA	60						
	Password Program (6)	2	XXX	A0	PWAx	PWDx								
	Password Read (7)	8	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3	04	PWD 4	05	PWD 5
			06	PWD 6	07	PWD 7								
	Password Unlock (7)	11	00	25	00	03	00	PWD 0	01	PWD 1	02	PWD 2	03	PWD 3
			04	PWD 4	05	PWD 5	06	PWD 6	07	PWD 7	00	29		
	Instruction Set Exit	2	XXX	90	XXX	00								
Global	PPB Instruction Set Entry	3	AAA	AA	55	55	AAA	C0						
	PPB Program	2	XXX	A0	SA	00								
	All PPB Erase	2	XXX	80	00	30								
	PPB Status Read	1	SA	RD(0)										
	PPB Instruction Set Exit	2	XXX	90	XXX	00								
Global	PPB Lock Instruction Set Entry	3	AAA	AA	555	55	AAA	50						
	PPB Lock Bit Set	2	XXX	A0	XXX	00								
	PPB Lock Status Read	1	XXX	RD(0)										
	PPB Lock Instruction Set Exit	2	XXX	90	XXX	00								
Volatile	DYB Instruction Set Entry	3	AAA	AA	555	55	AAA	E0						
	DYB Set	2	XXX	A0	SA	00								
	DYB Clear	2	XXX	A0	SA	01								
	DYB Status Read	1	SA	RD(0)										
	DYB Instruction Set Exit	2	XXX	90	XXX	00								

Legend
X = Don't care RD(0) = Read data.
SA = Sector Address. Address bits Amax–A16 uniquely select any sector. PWD = Password
PWDx = Password word0, word1, word2, and word3.

Data = Lock Register Contents: PD(0) = Secured Silicon Sector Protection Bit, PD(1) = Persistent Protection Mode Lock Bit, PD(2) = Password Protection Mode Lock Bit.

Note

1. All values are in hexadecimal.
2. All bus cycles are write cycles unless otherwise noted.
3. Data bits DQ15-DQ8 are don't cares for unlock and instruction cycles.
4. In each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.
5. Address bits A_{MAX}:A12 are don't cares for unlock and instruction cycles, unless SA or PA required. (A_{MAX} is the Highest Address pin.)
6. For PWDx, only one portion of the password can be programmed per each "A0" instruction.
7. Note that the password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.

4.2 Autoselect

4.2.1 Autoselect Addresses in System

Description	Address	Read Data (word/byte mode)
Manufacturer ID	00h	xx01h/1h
Device ID, Word 1	01h	227Eh/7Eh
Device ID, Word 2	0Eh	2248h/28h (BY29GM2GFS)
Device ID, Word 3	0Fh	2201h/01h
Secure Device Verify	03h	XX19h/19h = Not Factory Locked. XX99h/99h = Factory Locked.
Sector Protect Verify	(SA) + 02h	xx01h/01h = Locked, xx00h/00h = Unlocked

Note

1. *In each cycle of operation, the corresponding A26 address must be consistent to ensure the correct input of the instruction.*

5. AC Characteristics

5.1 Erase And Programming Performance

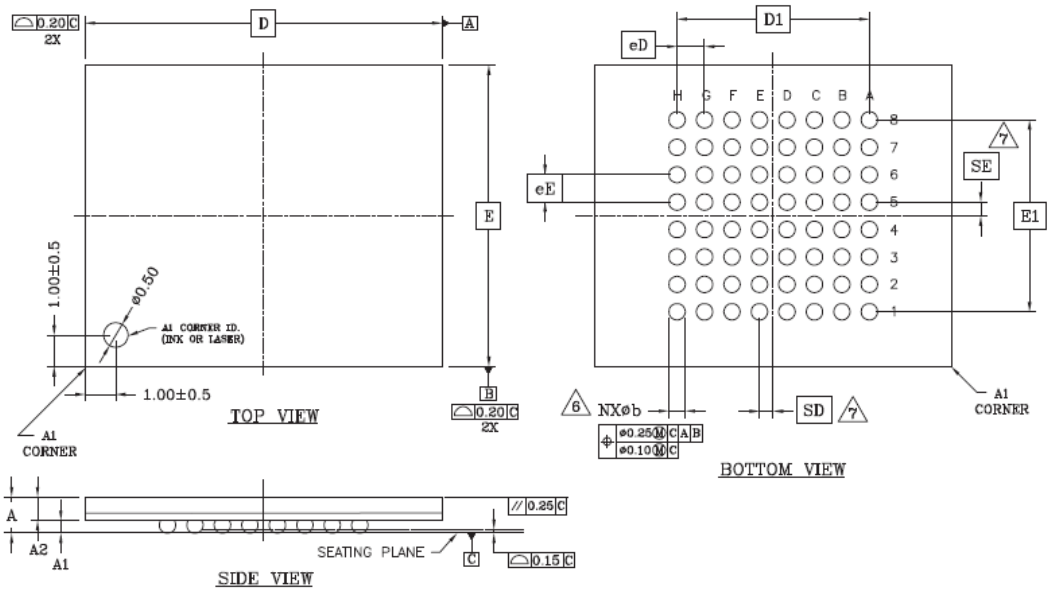
Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time	BY29GM2GFS	1024	4096	sec	
Total Write Buffer Time (Note 3)		480		µs	Excludes system level overhead (Note 5)
Total Accelerated Write Buffer Programming Time (Note 3)		432		µs	
Chip Program Time	BY29GM2GFS	1968		sec	

Note

1. *Typical program and erase times assume the following conditions: 25°C, 3.6 V V_{CC}, 10,000 cycles, checkerboard pattern.*
2. *Under worst case conditions of -40°C, V_{CC} = 3.0 V, 100,000 cycles.*
3. *Effective write buffer specification is based upon a 32-word write buffer operation.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program instruction.*

6. Package Information

6.1 BGA64(11x13mm)

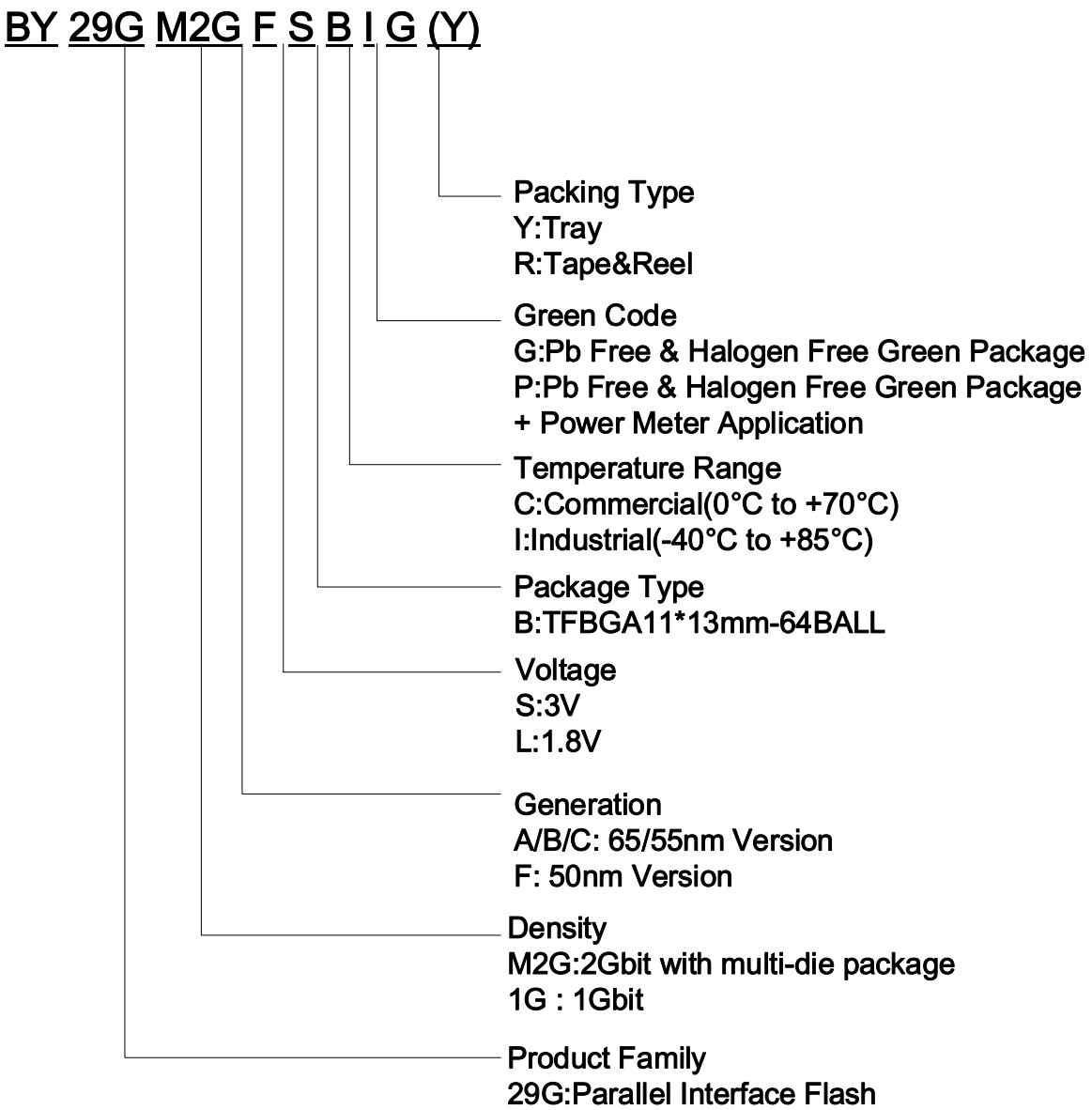


PACKAGE	LAA 064			
JEDEC	N/A			
	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE HEIGHT
A1	0.40	---	---	STANDOFF
A2	0.60	---	---	BODY THICKNESS
D		13.00 BSC.		BODY SIZE
E		11.00 BSC.		BODY SIZE
D1		7.00 BSC.		MATRIX FOOTPRINT
E1		7.00 BSC.		MATRIX FOOTPRINT
MD		8		MATRIX SIZE D DIRECTION
ME		8		MATRIX SIZE E DIRECTION
N		64		BALL COUNT
ϕb	0.50	0.60	0.70	BALL DIAMETER
eD		1.00 BSC.		BALL PITCH - D DIRECTION
eE		1.00 BSC.		BALL PITCH - E DIRECTION
SD / SE		0.50 BSC.		SOLDER BALL PLACEMENT
		NONE		DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010 (EXCEPT AS NOTED).
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW PARALLEL TO THE D OR E DIMENSION, RESPECTIVELY, SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. NOT USED.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

7. Order Information



8. Document Change History

Doc. Rev.	Tech Dev. Rev.	Effective Date	Change Description	Author
1.0		2020-05-08	Initiate;	BoyaMicro
1.1		2022-08-19	Add BGA64 package information	BoyaMicro